AMENDMENTS TO THE SPECIFICATION:

IN THE ABSTRACT:

Please replace the original page 51 with the accompanying replacement page 51, which includes the following rewritten paragraph beginning at page 51, line 2:

Encoder circuitry ~~(39)~~ for applying a low-density parity check (LDPC) code to information words is disclosed. The encoder circuitry ~~(39)~~ takes advantage of a macro matrix arrangement of the LDPC parity check matrix in which a left-hand portion of the parity check matrix is arranged as an identity macro matrix, each entry of the macro matrix corresponding to a permutation matrix having zero or more circularly shifted diagonals. The encoder circuitry ~~(39)~~ includes a cyclic multiply unit ~~(88)~~, which includes a circular shift unit ~~(104)~~ for shifting a portion of the information word according to shift values stored in a shift value memory ~~(82)~~ for the matrix entry, and a bitwise exclusive-OR function ~~(106)~~ for combining the shifted entry with accumulated previous values for that matrix entry. Circuitry ~~(92, 96)~~ for solving parity bits for row rank deficient portions of the parity check matrix is also included in the encoder circuitry ~~(39)~~.